

# TEC Preamp Shaper Power<sub>i</sub> Consumption:

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## Specifications:

Inputs: 32  
Outputs: 64 [1 De/Dx and 1 TR output per input]  
Number of TEC-PS Chips / board : 4  
Number of Line Drivers / board : 64

## Power Numbers:

### TEC-PS:

Current consumption per TEC-PS chip:

Vdd : 57 mA  
Vss<sub>ii</sub> : 52 mA

Current consumption per TEC-PS board:

Vdd : 228 mA  
Vss<sub>ii</sub> : 208 mA

### Line Drivers:

Quiescent Current per driver : 2.75 mA  
Total quiescent current per board : 176 mA

The Transmission Line is a 100 ohm system:

Case A: DeDx at its maximum output and TR at 1/5<sup>th</sup> of the DeDx output:  
1 channel:

DeDx @ MAX[+2.5 or -2.5] : 25 mA  
TR @ 1/5<sup>th</sup> of DeDx : 5 mA

32 Channel:

DeDx : 800 mA  
TR : 160 mA

Total current consumption in case A:  $I_{DeDx} + I_{TR} + I_q$

800 + 160 + 176  
Total Case A: 1136mA

Case B: DeDx at its maximum output and TR at its maximum<sub>iii</sub>:  
1 channel:

DeDx @ MAX[+2.5 or -2.5] : 25 mA  
TR @ MAX[+2.5 or -2.5] : 25 mA

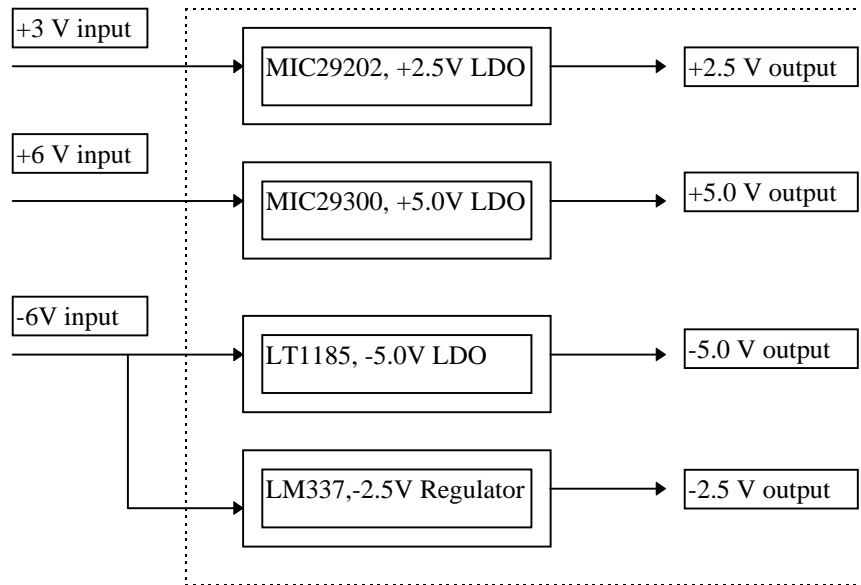
32 Channel:

DeDx : 800 mA  
TR : 800 mA

Total current consumption in case A:  $I_{DeDx} + I_{TR} + I_q$

800 + 800 + 176  
Total Case A: 1776mA

### Regulation Scheme:



Current required from the Unregulated supply<sub>iv</sub>:

$$\begin{aligned}
 +3 \text{ Volts} &: 228 \text{ mA} + 15 \text{ mA} &= 243 \text{ mA} \\
 +6 \text{ Volts} &: 2 (800 \text{ mA}) + 176 \text{ mA} + 35 \text{ mA} &= 1811 \text{ mA} \\
 -6 \text{ Volts} &: 2 (800 \text{ mA}) + 176 \text{ mA} + 208 \text{ mA} + 5 \text{ mA} &= 1989 \text{ mA}
 \end{aligned}$$

TEC-PS Front End current requirement:

Unregulated Supply	I <sub>peak</sub>	I <sub>quiescent</sub>	Units
+3V	243	243	mA
+6V	1811	211	mA
-6V	1989	389	mA

Notes:

- This power consumption numbers is not complete, as components like DAC and serial interface logic are not included.
- Actual current flow is  $I_{vdd} = 56.74 \text{ mA}$   
 $I_{vss} = 52.19 \text{ mA}$   
 $I_{gnd} = 4.55 \text{ mA}$   
 Ground current was neglected for simplicity.
- DeDx has a gain of 5 over the TR output, when TR goes to its maximum, DeDx will be clamped to its saturation output voltage.
- This Current includes the regulator current,  
 $+3V : I_{vdd,TECPS} + I_{reg}$   
 $+6V : I_{vcc,driver,DeDx} + I_{vcc,driver,TR} + I_{drivers,quiescent} + I_{reg}$   
 $-6V : I_{vee,driver,DeDx} + I_{vee,driver,TR} + I_{drivers,quiescent} + I_{vss,TECPS} + I_{reg}$